In the Claims:

Please amend claims 1-15 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A method of manufacturing a semiconductor device ~~(10)~~ comprising a substrate ~~(1)~~ and a semiconductor body ~~(2)~~ in which at least one semiconductor element is formed, wherein, in the semiconductor body ~~(2)~~, a semiconductor island ~~(3)~~ is formed by forming, in the surface of the semiconductor body ~~(1)~~, a first recess ~~(4)~~ the walls of which are covered with a dielectric layer (6), after which a lateral part of the semiconductor body ~~(2)~~ is removed by means of underetching via the bottom of the first recess, thereby forming a cavity ~~(20)~~ in the semiconductor body ~~(2)~~ above which the semiconductor island ~~(3)~~ is formed, and wherein a second recess ~~(5)~~ is formed in the surface of the semiconductor body, the walls of said second recess being covered with ~~a further~~ the dielectric layer, and one of the walls of the second recess ~~(5)~~ covered with the ~~further~~ dielectric layer being used to form a side wall of the semiconductor island ~~(3)~~, characterized in that ~~for both the dielectric layer and the further dielectric layer use is made of the same dielectric layer (6),~~ a lateral dimension of the second recess ~~(5)~~ and the thickness of the dielectric layer ~~(6)~~ being chosen such that the second recess ~~(5)~~ is filled substantially completely by the dielectric layer ~~(6)~~, and the lateral dimensions of the first recess ~~(4)~~ being chosen such that the walls and the bottom of the first recess ~~(4)~~ are provided with a uniform coating by the dielectric layer ~~(6)~~.

2. (Currently amended) A method as claimed in claim 1, characterized in that after the formation of the first and the second recesses ~~(4, 5)~~, the dielectric layer ~~(6)~~ is applied over the entire surface of the semiconductor body ~~(2)~~, after which the flat parts of the dielectric layer ~~(6)~~ are removed ~~again~~ by means of anisotropic etching.

3. (Currently amended) A method as claimed in claim 1, characterized in that the second recess ~~(5)~~ is formed as a ring-shaped groove ~~(5)~~ surrounding the first recess ~~(4)~~, within which groove the semiconductor island ~~(3)~~ is formed, the lateral dimension of the second recess ~~(5)~~ being formed by the width of the groove ~~(5)~~.

4. (Currently amended) A method as claimed in claim 1, characterized in that before the dielectric layer ~~(6)~~ is provided, ~~further~~ grooves ~~(7)~~ are formed in the surface of the semiconductor body ~~(2)~~, which have approximately the same width as the second recess ~~groove (5)~~, as a result of which the semiconductor island ~~(3)~~ is divided into semiconductor sub-islands ~~(3A)~~.

5. (Currently amended) A method as claimed in claim 4, characterized in that the shape of the second recess ~~groove (5)~~, viewed in projection, is square, and the ~~further~~ grooves ~~(7)~~ are formed so as to extend from the middle of the sides of the square to the first recess ~~(4)~~ situated in the center.

6. (Currently amended) A method as claimed in claim 1,chararacterized in that the semiconductor body ~~(2)~~ is formed by a semiconductor substrate ~~(1)~~ on which ~~two~~ first and second semiconductor layers, which are formed ~~(8, 9)~~ of ~~a~~ different semiconductor materials, are provided.

7. (Currently amended) A method as claimed in claim 6, characterized in that [[a]] the first semiconductor layer ~~(8)~~ of a mixed crystal of silicon and germanium is provided on ~~a silicon~~ the semiconductor substrate ~~(1)~~, and [[a]] the second semiconductor layer ~~(9)~~ of silicon is provided on the first semiconductor layer ~~thereon~~.

8. (Currently amended) A method as claimed in claim 6, characterized in that to form the cavity ~~(20)~~ in the semiconductor body ~~(2)~~ use is made of an etchant for silicon which is selective with respect to the semiconductor material of the first semiconductor layer ~~(8)~~.

9. (Currently amended) A method as claimed in claim 8, characterized in that after the formation of the cavity ~~(20)~~, the first semiconductor layer ~~(8)~~ is removed by means of an etchant which is selective with respect to the semiconductor material of the second semiconductor layer ~~(9)~~.

10. (Currently amended) A method as claimed in claim 8, characterized in that during the formation of the cavity ~~(20)~~, the etching of silicon is stopped as soon as the cavity ~~(20)~~ has reached the first semiconductor layer ~~(8)~~, after which the ~~latter~~ first semiconductor is selectively removed.

11. (Currently amended) A method as claimed in claim 1, characterized in that a lateral dimension of the cavity ~~(20)~~ is chosen to be so large that the cavity ~~(20)~~ in the semiconductor body ~~(2)~~ extends, in this lateral direction, at least as far as ~~or beyond~~ the second recess ~~(5)~~.

12. (Currently amended) A method as claimed in claim 1, characterized in that, in the semiconductor body ~~(2)~~, a further layer ~~(11)~~ is formed from a different semiconductor material than the ~~overlying~~ part ~~(12)~~ of the semiconductor body (2) in which the cavity ~~(20)~~ is formed.

13. (Currently amended) A method as claimed in claim 1, characterized in that after the formation of the cavity ~~(20)~~, the walls thereof are covered with a different dielectric layer ~~(30)~~.

14. (Currently amended) A method as claimed in claim 1, characterized in that after the formation of the cavity ~~(20)~~, this cavity is filled with a ~~preferably~~ high-ohmic material ~~(40)~~.

15. (Currently amended) A method as claimed in claim 13, characterized in that the cavity ~~(20)~~ is filled with polycrystalline silicon after the walls of the cavity are covered with the different dielectric layer.

16. (Previously presented) A semiconductor device obtained by means of a method as claimed in claim 1.